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10EE764

# Seventh Semester B.E. Degree Examination, Dec.2016/Jan.2017
# VLSI Circuits & Design

Time: 3 hrs. Max. Marks:100

**Note:** ***Answer FIVE full questions, selecting at least TWO questions from each part.***



## PART – A

1 a. Discuss Moore's law with graph. **(04 Marks)**

b. Outline the procedure of masking E-beam masks. Mention its advantages and different types of E-beam masks. **(08 Marks)**

c. With the help of necessary structures, explain the twin tub process of CMOS fabrication process. **(08 Marks)**

2 a. Discuss the Latch up condition in pwell CMOS process. **(10 Marks)**

b. Discuss the drain to source current $I_{ds}$ versus voltage $V_{ds}$ relationship for non saturated and saturated regions. **(10 Marks)**

3 a. List the colour, stick encoding, layers, mask layout encoding for single metal nMOS process. **(06 Marks)**

b. Draw the circuit symbols and stick diagram of nMOS inverters and CMOS Inverters. **(08 Marks)**

c. Draw the stick diagram and layout plan for nMOS shift register cell. **(06 Marks)**

4 a. What is sheet resistance? Calculate sheet resistance of a transistor channel if L = 8λ, w = 2λ if n transistor channel $R_s = 10^4\Omega$/square. **(06 Marks)**

b. Derive the expression for rise time and fall time estimation of CMOS inverter delay. **(06 Marks)**

c. Write a note on BiCMOS drivers. **(08 Marks)**

## PART – B

5 a. Draw scaled nMOS transistor diagram. **(04 Marks)**

b. Indicate the scaling factors for any 10 transistor parameters. **(10 Marks)**

c. What are the limitations of sub threshold current and current density? **(06 Marks)**

6 a. Explain nMOS 4 bit dynamic shift register logic. **(05 Marks)**

b. What are the guidelines of a subsystem design process? **(05 Marks)**

c. Explain the structured design of bus arbitration logic for n lines. Also write the circuit diagram and stick diagram for a single cell. **(10 Marks)**

7 a. Explain with the neat diagram 4×4barrel shifter. **(10 Marks)**

b. Explain the general arrangement of 4 bit arithmetic processor. **(10 Marks)**

8 a. Explain the design of 4 bit adder with adder element requirements. **(10 Marks)**

b. Draw the structure of multiplexer based adder logic with stored and buffered sum output. **(10 Marks)**

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